IN THE CLAIMS:

1. (Withdrawn) A method of making an integrated circuit having a device layer of semiconductor above an array insulating layer and containing an array of DRAM cells including a trench capacitor connected by a buried strap to a pass transistor formed in said device layer, comprising the steps of:

forming said set of trench capacitors by etching trenches through said device layer and array insulating layer and depositing center electrodes insulated by a capacitor insulator;

recessing said center electrodes below a bottom surface of said device layer;

etching laterally into said array insulating layer outside said trenches, thereby exposing a contact area on said bottom surface of said device layer;

depositing strap conductive material in said trenches to a level above said bottom surface of said device layer, whereby said strap conductive material makes electrical contact with said bottom surface to form said buried straps;

depositing top insulating material having a top insulator thickness in said trenches above said strap conductive material; and

forming a set of cell pass transistors in said device layer having cell electrodes, transistor gates and internal electrodes in contact with said buried straps.

2. (Withdrawn) A method according to claim 1, further comprising a step of:

forming a first subset of interconnect lines contacting transistor gates in a first subset of cells and extending over trenches in a second subset of cells, said first subset of interconnect lines being separated vertically from said center electrodes in said second subset of cells by said top insulator thickness; and

forming a second subset of interconnect lines contacting transistor gates in said second subset of cells and extending over trenches in said first subset of cells, said second subset of interconnect lines being separated vertically from said center electrodes in said first subset of cells by said top insulator thickness.

3. (Withdrawn) A method according to claim 1, further comprising a step of removing said strap conductive material in said trenches to a level below said bottom surface of said device layer, whereby said strap conductive material makes contact with said device layer only on said bottom surface.

4. (Withdrawn) A method according to claim 1, further comprising a step of planarizing said top insulator layer and forming a set of isolating trenches by removing said device layer and said array insulating layer outside said trenches and said cell pass transistors, to a depth of at least said bottom of said device layer, whereby only that portion of said buried strap inside said trenches and underneath said transistors remains.

5. (Withdrawn) A method according to claim 2, further comprising a step of planarizing said top insulator layer and forming a set of isolating trenches by removing said device layer and said array insulating layer

outside said trenches and said cell pass transistors, to a depth of at least said bottom of said device layer, whereby only that portion of said buried strap inside said trenches and underneath said transistors remains.

6. (Withdrawn) A method according to claim 1, in which said step of etching laterally is performed by a substantially isotropic etch using fluorine chemistry.

7. (Withdrawn) A method according to claim 1, in which said array device layer has a thickness less than 100nm.

8. (Withdrawn) A method according to claim 1, in which said top insulator has a thickness greater than 100nm.

9. (Withdrawn) A method of making an integrated circuit having a device layer of semiconductor above an array insulating layer and containing an array of DRAM cells including a trench capacitor connected by a buried strap to a pass transistor formed in said device layer, comprising the steps of:

forming said set of trench capacitors by etching trenches through said device layer and array insulating layer and depositing center electrodes insulated by a capacitor insulator;

recessing said center electrodes below a bottom surface of said device layer;

etching laterally into said array insulating layer outside said trenches, thereby exposing a contact area on said bottom surface of said device layer;

depositing a conformal liner of conductive material in said trenches to a level above said bottom surface of said device layer, whereby said liner of conductive material makes electrical contact with said bottom surface;

depositing strap conductive material in said trenches to a level above said bottom surface of said device layer, whereby said strap conductive material makes an electrical path through said conformal liner of conductive material to form said buried straps;

depositing top insulating material having a top insulator thickness in said trenches above said strap conductive material; and

forming a set of cell pass transistors in said device layer having cell electrodes, transistor gates and internal electrodes in contact with said buried straps.

10. (Withdrawn) A method according to claim 9, further comprising a step of removing said strap conductive material in said trenches to a level below said bottom surface of said device layer, whereby said strap conductive material makes contact with said device layer only on said bottom surface.

11. (Withdrawn) A method according to claim 9, further comprising a step of planarizing said top insulator layer and forming a set of isolating trenches by removing said device layer and said array insulating layer outside said trenches and said cell pass transistors, to a depth of at least said bottom of said device layer, whereby only that portion of said buried strap inside said trenches and underneath said transistors remains.

12. Withdrawn) A method according to claim 9, in which said step of etching laterally is performed by a substantially isotropic etch using fluorine chemistry.

13. (Currently Amended) An integrated circuit having a device layer of semiconductor with a device layer thickness of less than 100nm above an array insulating layer and containing an array of DRAM cells including a trench capacitor connected by a buried strap to a horizontal pass transistor formed in said device layer, said pass transistor having an internal contact adjacent said trench, in which:

said set of trench capacitors have center electrodes insulated by a capacitor insulator, said center electrodes having a top surface below a bottom surface of said device layer;

said buried strap is formed from strap conductive material extending vertically in said trenches to a level below said bottom surface of said device layer and laterally outside said trenches and underneath said internal contact of said pass transistor, whereby said strap conductive material makes electrical contact with said bottom surface to form said buried straps; and

top insulating material having a top insulator thickness extending up to a surface of said device layer in said trenches ~~extending~~ above said strap conductive material and abutting a vertical surface of said internal contact of said pass transistor.

14. (Original) An integrated circuit according to claim 13, further having a conformal layer of conductive material extending along a top surface of said center electrode and said bottom surface of said device layer.

15. (Withdrawn) A method according to claim 9, further comprising a step of:

forming a first set of wordlines contacting transistor gates in said first subset of cells and extending as passing wordlines over trenches in said second subset of cells, said first set of wordlines passing over and being separated vertically from said buried straps in said second subset of cells by said top insulator thickness; and

forming a second set of wordlines contacting transistor gates in said second subset of cells and extending as passing wordlines over trenches in said first subset of cells, said second set of wordlines being separated vertically from said buried straps in said first subset of cells by said top insulator thickness.

16. (New) An integrated circuit having a device layer of semiconductor with a device layer thickness of less than 100nm above an array insulating layer and containing an array of DRAM cells disposed in a first subset of DRAM cells and a second subset of DRAM cells, including a trench capacitor formed at an edge of said DRAM cells and connected by a buried strap to a horizontal pass transistor formed in said device layer and displaced laterally from said trench capacitor, comprising:

said set of trench capacitors extending through said device layer and array insulating layer and having center electrodes insulated by a capacitor insulator;

said center electrodes being recessed below a bottom surface of said device layer;

a contact area on said bottom surface of said device layer outside said trenches;

strap conductive material disposed in said trenches to a level above said bottom surface of said device layer, whereby said strap conductive material makes electrical contact with said bottom surface to form said buried straps;

top insulating material having a top insulator thickness extending up to a surface of said device layer in said trenches above said strap conductive material, whereby said top insulator thickness is approximately equal to said device layer thickness; and

a set of isolating trenches extending through said device layer and said array insulating layer outside said trenches and said cell pass transistors, to a depth of at least said bottom of said buried straps, whereby only that portion of said buried strap inside said trenches and underneath said transistors remains and said buried straps are isolated from corresponding buried straps in adjacent cells by said isolating trenches;

a set of horizontal cell pass transistors in said device layer having cell electrodes, transistor gates disposed above said device layer and connected to a first subset of interconnect lines and internal electrodes in contact with said buried straps through said contact area and separated from an adjacent trench by said isolating trenches.

17. (New) An integrated circuit according to claim 16, further comprising:

a first subset of interconnect lines contacting transistor gates in said first subset of cells and extending over trenches in said second subset of cells, said first subset of interconnect lines passing over and being separated vertically from said buried straps in said second subset of cells by said top insulator thickness; and

a second subset of interconnect lines contacting transistor gates in said second subset of cells and extending over trenches in said first subset of cells, said second subset of interconnect lines being separated vertically from said buried straps in said first subset of cells by said top insulator thickness.

18. (New) An integrated circuit according to claim 16, in which said strap conductive material in said trenches is disposed only below said bottom surface of said device layer, whereby said strap conductive material makes contact with said device layer only on said bottom surface and said top insulating material has a top insulator thickness greater than said device layer thickness.

19. (New) An integrated circuit having a device layer of semiconductor with a device layer thickness of less than 100nm above an array insulating layer and containing an array of DRAM cells disposed in a first subset of

DRAM cells and a second subset of DRAM cells, including a trench capacitor formed at an edge of said DRAM cells and connected by a buried strap to a horizontal pass transistor formed in said device layer and displaced laterally from said trench capacitor, said array of DRAM cells having at least some pairs of cells having a trench capacitor in a first cell separated by a portion of material from a corresponding trench capacitor in an adjacent cell, comprising:

said set of trench capacitors extending trenches through said device layer and array insulating layer and having center electrodes extending below a bottom surface of said device layer and insulated by a capacitor insulator;

a conformal liner of conductive material disposed in said trenches to a level above said bottom surface of said device layer, whereby said liner of conductive material makes electrical contact with a bottom surface of said device layer at the location where said buried strap meets said buried surface;

strap conductive material disposed in said trenches to a level above said bottom surface of said device layer, whereby said strap conductive material makes electrical contact with said bottom surface to form said buried straps;

top insulating material having a top insulator thickness extending up to a surface of said device layer in said trenches above said strap conductive material, whereby said top insulator thickness is approximately equal to said device layer thickness; and

a set of isolating trenches extending through said device layer and said array insulating layer outside said trenches and said cell pass transistors, to a depth of at least said bottom of said buried straps, said isolating trenches being filled with an isolating material, whereby only that portion of said buried strap inside said trenches and underneath said transistors remains and said buried straps are isolated from corresponding buried straps in adjacent cells by said isolating material, and whereby said pairs of cells having a trench capacitor in a first cell separated by a portion of material from a corresponding trench capacitor in an adjacent cell are separated by said isolating material, so that the space available for passing wordlines comprises top insulators in said pairs of cells and said isolating trench;

a set of horizontal cell pass transistors in said device layer having cell electrodes, transistor gates disposed above said device layer and connected to a first subset of interconnect lines and internal electrodes in contact with said buried straps through said contact area and separated from an adjacent trench by said isolating trenches.

20. (New) An integrated circuit according to claim 19, further comprising strap conductive material disposed in said trenches to a level below said bottom surface of said device layer, whereby said strap conductive material makes contact with said device layer only on said bottom surface and said top insulating material has a top insulator thickness greater than said device layer thickness.

21. (New) An integrated circuit according to claim 19, further comprising:

a first set of wordlines contacting transistor gates in said first subset of cells and extending as passing wordlines over trenches in said second subset of cells, said first set of wordlines passing over and being separated vertically from said buried straps in said second subset of cells by said top insulator thickness; and

a second set of wordlines contacting transistor gates in said second subset of cells and extending as passing wordlines over trenches in said first subset of cells, said second set of wordlines being separated vertically from said buried straps in said first subset of cells by said top insulator thickness.